WHAT IS CLAIMED IS:

1. A memory controller in an adaptable computing machine (ACM), the controller comprising:

a network interface configured to receive a memory request from a programmable network; and

a memory interface configured to access a memory to fulfill the memory request from the programmable network,

wherein the memory interface receives and provides data for the memory request to the network interface, the network interface configured to send data to and receive data from the programmable network.

2. The controller of claim 1, further comprising one or more engines, the one or more engines configured to provide memory access services.

3. The controller of claim 2, wherein the memory access services comprise at least one of a peek/poke service, a memory random access service, a point-to-point service, a direct memory access service, a messaging service and a real-time input service.

4. The controller of claim 1, wherein the memory comprises at least one of a SDRAM interface and a flash memory interface.

5. The controller of claim 1, wherein the network interface provides flow control with a node that has sent the memory request.

6. A memory controller in an adaptable computing machine (ACM), the controller comprising:

a network interface configured to receive a memory request for a memory access service from a network; and

one or more engines configured receive the memory request and to provide the memory access service associated with the memory request.

7. The controller of claim 6, wherein the one or more engines comprise a peek/poke engine, a memory random access engine, a point-to-point engine, a direct memory access engine, and a real-time input engine.

8. The controller of claim 6, wherein the memory access service comprises at least one of a peek/poke service, a memory random access service, a point-to-point service, a direct memory access service, a messaging service and a real-time input service.

9. The controller of claim 6, wherein the network interface provides flow control with a node that has sent the memory request.

10. A memory controller in an adaptable computing machine (ACM), the controller comprising:

one or more ports configured to receive memory requests, wherein each port includes one or more parameters;

an engine configured to receive a memory request from a port in the one or more ports; and

a data address generator configured to generate a memory location for a memory based on the one or more parameters associated with the port,

wherein the engine is configured to perform a memory operation for the memory request using the generated memory location.

11. The controller of claim 10, wherein the engine comprises an engine to perform at least one of point-to-point memory requests, direct memory access memory requests, and real-time input memory requests.

12. The controller of claim 10, wherein the data address generator is configured by the one or more parameters associated with the port.

13. The controller of claim 10, wherein the memory operation comprises at least one of a read and a write operation.

14. The controller of claim 10, wherein the memory location comprises one or more addresses.

15. The controller of claim 10, wherein the data address generator uses an initial location determined from the memory request to determine the memory location.

16. The controller of claim 15, wherein the initial location comprises a base address and an offset is used to determine the memory location.

17. The controller of claim 10, wherein the engine is configured to perform the memory operation while conforming to a point-to-point protocol with a requesting node that sent the memory request.

18. A memory controller in an adaptable computing machine (ACM), the node comprising:

one or more ports configured to receive memory requests from requesting nodes, wherein each port includes one or more parameters, the one or more parameters configurable by information in the memory requests;

a point-to-point engine configured to receive a memory request from a port in the one or more ports;

a data address generator configured to generate a memory location for a memory based on the one or more parameters associated with the port,

wherein the point-to-point engine performs a memory operation using the generated memory location while adhering to a point-to-point protocol with the requesting node.

19. The controller of claim 18, wherein the memory request comprises at least one of a data request and a control request,

wherein the data request includes data to be written and the control request includes information usable to update the one or more parameters.

20. The controller of claim 19, wherein the control request is included in a control word and the data request is included in a data word.

21. The controller of claim 19, wherein the control request includes data usable for configuring the one or more parameters associated with the port.

22. The controller of claim 21, wherein the control request includes an indication to perform a read after the one or more parameters have been configured.

23. The controller of claim 18, wherein the memory request includes a data request that includes data to be written in a memory.

24. The controller of claim 23, wherein the data is written into the memory using the one or more parameters associated with the port.

25. The controller of claim 24, wherein the memory location generated by the data address generator is used to write or read the data at that memory location in the memory.

26. The controller of claim 18, wherein the point-to-point engine and requesting node communicate using forward and backward ACKs to maintain flow control.

27. A system for processing memory service requests in an adaptable computing environment, the system comprising:

a memory;

one or more nodes configured to generate a memory service request;

a memory controller configured to receive the memory service request, the memory controller configured to service the memory service request, wherein the memory controller reads or writes data from or to the memory based on the memory service request.

28. The system of claim 27, wherein the memory controller provides at least one of the following services: a peek/poke service, a memory random access service, a point-to-point service, a direct memory access service, a messaging service and a real-time input service.

29. The system of claim 27, wherein the memory comprises at least one of a SDRAM and Flash memory.

30. The system of claim 27, wherein the one or more nodes comprise an adaptable computing node.

31. The system of claim 27, wherein the memory controller comprises one or more ports, wherein each port in the one or more ports includes one or more parameters.

32. The system of claim 31, wherein the memory controller comprises a data address generator, the data address generator configured to use the one or more parameters associated with a port in the one or more ports to determine a location in the memory to read or write data.